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Publication

1. Paresh Kumar Pasayat, Janmejaya Rout, Kodanda Dhar Sa,” FPGA Based Implementation of Encryption and Decryption Of 16-Bit Data Using VHDL”, IJERT, vol. 2, pp. 1188-1192, 2013.

2. Paresh Kumar Pasayat, Manoranjan Pradhan, Bhupesh Kumar Pasayat,” FPGA based implementation of 8-bit ALU of a RISC processor using Booth algorithm written in VHDL language”, IJERT, vol. 2, pp. 1386-1393, 2013.

3. Sonam Barik, Paresh Kumar Pasayat, "Design and Implementation of Hamming Code Technique Used for providing security to 128-bit Digital Data with Error Detection and Correction written in VHDL Code", IJAREEIE, vol. 5, pp. 6007-6011, 2016.
4. Paresh Kumar Pasayat, Sonam Barik, "Design and implementation of transmission of 128-bit digital data generated from a data generation unit from one base station to another base station with its reception at the receiver end using "Hamming (224,128) Code technique" written in VHDL code", IJRASET, vol. 4, pp. 476-482, 2016.
5. Paresh Kumar Pasayat, RajshreeNath, BipashaPradhan, Anil Kumar Dakua, Swadhyaya Mohanty, Abhinav Das," Design and implementation of combined effect of modified DES and Hamming (224,128) Code data security techniques on the transmission of 128-bit digital data from one base station to another base station written in VHDL", IRJET, vol. 3, pp. 322-325,2016.
6. Paresh Kumar Pasayat, Sony Naik, "Simulation based design and analysis of combined effect of various data security techniques used during the transmission of 128-bit digital data generated from 128-bit data generation unit written in VHDL Code using Xilinx ISE 9.2i software", IRJET, vol. 4, pp. 245-250, 2017.
7. Paresh Kumar Pasayat, Kalpataru Sethi, "Effect of newly developed data security algorithm on the 128-bits plaintext and study of resistance to ciphertext attacks with maximum combinational path delay using VHDL", IRJET, Vol. 5, pp.1652-1653, 2018.
8. Anwesha Das, Paresh Kumar Pasayat, "Design and implementation of 256-bit symmetric key cryptography algorithm used in the data security written in VHDL", IRJET, vol. 6, pp.526-527, 2019.
9. Anwesha Das, Paresh Kumar Pasayat, "Design and Implementation of 256-bits Cryptography Algorithm used in the Data Security with Resistance to Brute-Force and Timing Attacks Written in VHDL code using Xilinx ISE 9.2i Software", IRJET, vol. 6, pp. 1848-1851, 2019.

10. Gyanaranjan Samal, Paresh Kumar Pasayat, "Enhancement of 128-bits Data Security through Steganography and Cryptography Techniques", vol. 6, pp.378-379, 2019.
11. Paresh Kumar Pasayat, B Manoranjan Patra, Madhusmita Das, Ayan Lodh, Barsha Baisakhi Priyadarshini, Ashis Kumar Samal, Monalisha Sethi, "Design and Implementation of 256-bits Data Security Algorithm Written in VHDL Code with Data Integrity Test", IJAREEIE, vol. 10, Issue 3, pp.843-846, 2021.
12. Paresh Kumar Pasayat, Ayan Lodh, Madhusmita Das, B Manoranjan Patra, Barsha Baisakhi Priyadarshini, Ashis Kumar Samal, Monalisha Sethi, "Design and Implementation of 256-bits Hybrid Data Security Algorithm Written in VHDL Code with Data Integrity Test", IJAREEIE, vol. 10, Issue 5, pp.1447-1451, 2021.
13. Paresh Kumar Pasayat, Soumya Ranjan Panigrahi, Chandan Kumar Padhy, Manaswini Mishra, Trupti Mishra, Ajay Kumar Manadhata, "Design and Analysis of Complex Data Security Algorithm Using Cryptography and Steganography Techniques", IJIRCCE, vol. 9, Issue 12, pp.14828-14831, 2021.