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**Publication:**

## A. International Journals


1. E. Mohapatra, **T. P. Dash**, S. Das, D. Jena, and C. K. Maiti, "Design and Optimization of Stress/Strain in GAA Nanosheet FETs for Improved FOMs at Sub-7nm Nodes," Physica Scripta, vol. 98, p.065919, 2023 (IOP Publisher, I.F. 3.081, SCI Indexed), **DOI:** https://doi.org/10.1088/1402-4896/accfcc

2. D. Jena, S. Das and **T. P. Dash**, "Design and Simulation of Enhancement-Mode Vertical Superjunction GaN HEMT with Improved Ron and Cut-off Frequency," IETE Journal of Research, pp.1-9, 2023. (Taylor & Francis Publisher, I.F. 1.500, SCI Indexed), DOI: https://doi.org/10.1080/03772063.2023.2271429

3. D. Jena, S. Das, E. Mohapatra, and **T.P. Dash**, "Linearity Improvement in Graded Channel AlGaN/GaN HEMTs for High-Speed Applications," Physica Scripta, vol. 98, p.065919, 2023 (IOP Publisher, I.F. 3.081, SCI Indexed), **DOI:** https://doi.org/10.1088/1402-4896/acf3b6

4. E. Mohapatra, **T. P. Dash**, S. Das, D. Jena, and C. K. Maiti, "Work function variability and inverter design possibility in advanced gate all around FETs, " Nanomaterials and Energy, vol. 12 (2), pp. 81-89, 2023. (ICE Publisher, I.F. 1.100, ESCI), DOI: https://doi.org/10.1680/jnaen.23.00029

5. J. Jena, D. Jena, E. Mohapatra, S. Das, and **T. P. Dash**, "FinFET-based Inverter Design and Optimization at 7nm Technology Node," Silicon, vol. 14 pp. 10781–10794, 2022. (Springer Publisher, **SCI, I.F: 2.474**) https://doi.org/10.1007/s12633-022-01812-6

6. D. Jena, S. K Palo, A. K. Panda, **T. P. Dash**, T. Sahu, "Nonlinear electron mobility due to asymmetric doping in V-shaped double quantum well FET structure," Indian Journal of Physics, vol. 96, pp. 4185-4191 2022. ( Springer Publisher, **SCI, IF: 1.947**,). https://doi.org/10.1007/s12648-022-02366-4

7. P.P. Maiti, A. Dash, S. Guhathakurata, A Bag, S. Das, **T. P. Dash**, G. Ahmad, C. K. Maiti, and S Mallik, "Experimental and simulation study of charge transport mechanism in $HfTiO_x$ high-*k* gate dielectric on SiGe heterolayers". *Bull Mater Sci,* vol.45, Springer, 2022. (**SCI, I.F.: 1.878)**. https://doi.org/10.1007/s12034-021-02622-z

8. **T. P. Dash**, E. Mohapatra, and C. K. Maiti, "Deformation-induced stress/strain mapping and performance evaluation of a-IGZO thin-film transistors for flexible electronic applications," J Soc Inf Display., vol. 29, pp.130–142, 2020; (Wiley Publisher **I. F:1.645, SCI Indexed**). DOI: https://doi.org/10.1002/jsid.963

9. S. Das, **T.P. Dash**, D. Jena, E. Mohapatra, C. K. Maiti, "Strain-Engineering in AlGaN/GaN HEMTs: Impact of Silicon Nitride Passivation Layer on Electrical Performance", Physica Scripta, vol. 96, p.124074, **2021**. (**IOP Publisher, I.F. 2.151, SCI Indexed**) https://doi.org/10.1088/1402-4896/ac3ef9

10. E. Mohapatra, **T. P. Dash**, J. Jena, S. Das, and C. K. Maiti, "Design study of gate-all-around vertically stacked nanosheet FETs for sub-7nm nodes," SN Appl. Sci. 2021 35, vol. 3, no. 5, pp.1–13, 2021. (Springer Publisher, JCI: 0.32) DOI: https://doi.org/10.1007/s42452-021-04539-y

11. J. Jena, **T.P. Dash**, S. Das, E. Mohapatra, S. Das, and J. Nanda, "Process Induced Stress Optimization for Compressively Stressed p-Channel FinFET at 7N," International Journal of High-Speed Electronics and Systems, vol. 10, 2022. (World Scientific Publisher, Scopus Indexed). https://doi.org/10.1142/S012915642140005X

12. **T. P. Dash**, S. Dey, S. Das, E. Mohapatra, J. Jena, and C. K. Maiti, "Strain-Engineering in Nanowire Field-Effect Transistors at 3nm Technology Node," *Phys. E Low-dimensional Syst. Nanostructures*, vol. 118, p. 113964, Apr. 2020. (**Elsevier Publisher, I. F=3.176, SCI indexed**) DOI: https://doi.org/10.1016/j.physe.2020.113964

13. S. Dey, J. Jena, E. Mohapatra, **T. P. Dash**, S. Das and C. K. Maiti, "Design and Simulation of Vertically-Stacked Nanowire Transistors at 3nm Technology Nodes," Physica Scripta, vol. 95, p. 014001, 2019. IOP Publisher. (**IOP Publisher, I.F. 2.151, SCI Indexed**). DOI: https://doi.org/10.1088/1402-4896/ab4621

14. E Mohapatra, T P Dash, J Jena, S Das and C K Maiti, "Strain induced variability study in Gate-All-Around vertically-stacked horizontal nanosheet transistors," Physica Scripta, vol, 95, p. 065808 2020, DOI: https://doi.org/10.1088/1402-4896/ab89f5

15. **T. P. Dash**, J. Jena, E. Mohapatra, S. Dey, S. Das, and C. K. Maiti, "Role of Stress/Strain Mapping and Random Dopant Fluctuation in Advanced CMOS Process Technology Nodes," International Journal of Nano and Biomaterials (IJNBM), vol. 9, pp. 18-33, 2020. (Inderscience Publishers). DOI: https://dx.doi.org/10.1504/IJNBM.2020.107413

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17. **T. P. Dash**, S. Dey, S. Das, J. Jena, E. Mahapatra, and C. K. Maiti, "Source/Drain Stressor Design for Advanced Devices at 7nm Technology Nodes," Nanoscience & Nanotechnology-Asia, vol. 10, pp.447 – 456, 2020. (Bentham Science Publishers). DOI: https://doi.org/10.2174/2210681209666190809101307

18. E. Mohapatra, **T. P. Dash**, J. Jena, S. Dey, S. Das and C. K. Maiti "Vertically-Stacked Silicon Nanosheet Field Effect Transistors at 3nm Technology Nodes – Simulation at Nanoscale," International Journal of Nanoparticle (IJNP), vol.12, pp.224 – 237, 2020. (Inderscience Publisher) DOI: https://doi.org/10.1504/IJNP.2020.109546

19. **T. P. Dash**, S. Dey, S. Das, J. Jena, E. Mohapatra, and C. K. Maiti, "Performance Comparison of Strained-SiGe and Bulk-Si Channel FinFETs at 7N Technology Node," Journal of Micromechanics

and Microengineering, vol. 29, p. 104001, 2019. (IOP Publisher, **I.F. 2.141**, **SCI Indexed**). DOI: https://doi.org/10.1088/1361-6439/ab31c8

20. **T. P. Dash**, J. Jena, E. Mohapatra, S. Dey, S. Das, and C. K. Maiti, "Stress-induced Variability Studies in Tri-Gate FinFETs with Source/Drain Stressor at 7nm Technology Nodes," Journal of Electronic Materials, vol. 48, pp.5348-5362, 2019. (Springer Publisher, **I.F 1.676**, **SCI Indexed**). DOI: https://doi.org/10.1007/s11664-019-07348-7.

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28. D. Pradhan, S. Das, and **T. P. Dash**, "Study of strained-Si p-channel MOSFETs with HfO2 gate dielectric," Superlattices and Microstructures, vol. 98, pp. 203-207, 2016. (Elsevier Publisher, **SCI Indexed, I.F. 2.385**) DOI: https://doi.org/10.1016/j.spmi.2016.08.019

29. F.A. Ali, A. Sahoo, **T. P. Dash** and G. Bose, "Study of 65 nm n-MOSFET Using SILVACO TCAD", Advanced Science Letters, vol. 22, 2, 2016, pp. 381-383, DOI: https://doi.org/10.1166/asl.2016.6850

## B. Book Chapters:

1. **T.P. Dash**, C.K. Maiti, An overview of nanoscale device fabrication technology—part I In: Nanoelectronics: Physics, Materials and Devices, ch 9, pp. 169 – 223, Elsevier. https://doi.org/10.1016/B978-0-323-91832-9.00007-5

2. S. Das, **T.P. Dash**, B. Baral, S. M. Biswal, D. Jena and E. Mohapatra, Analytical modeling of nanoscale advance devices and their reliability aspects. In: Nanoelectronics: Physics, Materials and Devices ch 15, pp. 385-408, 2023, Elsevier. https://doi.org/10.1016/B978-0-323-91832-9.00011-7

3. **T. P. Dash**, Bulk-Si FinFETs. In: Stress and Strain Engineering at Nanoscale in Semiconductor Devices. C. K. Maiti, Ed. , NY: CRC Press, ch. 5, pp. 135-168, 2021. ISBN 9780367519292. https://www.routledge.com/Stress-and-Strain-Engineering-at-Nanoscale-in-Semiconductor-Devices/Maiti/p/book/9780367519292

4. **T. P. Dash**, Strain-Engineered FinFETs at NanoScale. In: Stress and Strain Engineering at Nanoscale in Semiconductor Devices. C. K. Maiti, Ed. , NY: CRC Press, ch. 6, pp. 169-194, 2021. ISBN 9780367519292. https://www.routledge.com/Stress-and-Strain-Engineering-at-Nanoscale-in-Semiconductor-Devices/Maiti/p/book/9780367519292

5. **T. P. Dash**, E. Mohapatra, S. Das , S. Choudhury , C.K. Maiti , Toward Ultimate Scaling: From FinFETs to Nanosheet Transistors. In: R. Sharma, M. Mishra, J. Nayak, B. Naik, D. Pelusi (eds) Green Technology for Smart City and Society. Lecture Notes in Networks and Systems, vol 151. Springer, Singapore,2021. https://doi.org/10.1007/978-981-15-8218-9_19

6. E. Mohapatra, **T. P. Dash**, J. Jena, S. Das, J. Nanda, C.K. Maiti (2020) Performance Analysis of Si-Channel Nanosheet FETs with Strained SiGe Source/Drain Stressors. In: G. Pradhan, S. Morris, N. Nayak (eds) Advances in Electrical Control and Signal Systems, Lecture Notes in Electrical Engineering, vol 665., pp 329-337, Springer, Singapore, 2020. https://doi.org/10.1007/978-981-15-5262-5_23

7. J. Jena, **T. P. Dash**, E. Mohapatra, S. Das, J. Nanda, C.K. Maiti (2020) Modeling and Performance Analysis of n-FinFETs: A Comparative Study. In: Pradhan G., Morris S., Nayak N. (eds) Advances in Electrical Control and Signal Systems, Lecture Notes in Electrical Engineering, vol 665. pp 765-776 Springer, Singapore,2020. https://doi.org/10.1007/978-981-15-5262-5_57

8. R.K. Nanda, E. Mohapatra, **T. P. Dash**, P. Saxena, P. Srivastava, R. Trigutnayat, C. K. Maiti (2020) Atomistic Level Process to Device Simulation of GaNFET Using TNL TCAD Tools. In: Pradhan G., Morris S., Nayak N. (eds) Advances in Electrical Control and Signal Systems, Lecture Notes in Electrical Engineering, vol 665. pp 815-826, Springer, Singapore, 2020. https://doi.org/10.1007/978-981-15-5262-5_61

9. **T. P. Dash**, S. Dey, S. Das, J. Jena, and C. K. Maiti Stress Profile Analysis in n-FinFET Devices. In: Mandal J., Bhattacharya D. (eds) Emerging Technology in Modelling and Graphics. Advances in Intelligent Systems and Computing, vol 937. Springer, Singapore, 2020. https://doi.org/10.1007/978-981-13-7403-6_29

10. S. Das, **T. P. Dash**, C. K. Maiti, Low Frequency Noise Analysis in Strained-Si Devices. In: Mandal J., Bhattacharya D. (eds) Emerging Technology in Modelling and Graphics. Advances in Intelligent Systems and Computing, vol 937. Springer, Singapore, 2020. https://doi.org/10.1007/978-981-13-7403-6_37

11. **T. P. Dash**, S. Das, R. K. Nanda, Silicon–Germanium Channel Heterostructure p-MOSFETs. In: Nath V. (eds) Proceedings of the International Conference on Microelectronics, Computing & Communication Systems. Lecture Notes in Electrical Engineering, vol. 453. pp. 365-374, Springer, Singapore, 2017. https://doi.org/10.1007/978-981-10-5565-2_32

12. S. Das, **T. P. Dash**, R. K. Nanda, and C. K. Maiti, Study of Strained-Si/SiGe Channel p-MOSFETs Using TCAD. In: Nath V. (eds) Proceedings of the International Conference on Microelectronics, Computing & Communication Systems. Lecture Notes in Electrical Engineering, vol. 453.pp. 181-188, Springer, Singapore, 2017. https://doi.org/10.1007/978-981-10-5565-2_16

## C. International Conferences:

1. D. Jena, S. Das, A. Tripathy and T. Dash, "Comparative Study of AlGaN/GaN-Based Polarization Junction Super HFET," 2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS), Bhubaneswar, India, 2023, pp. 1-6, doi: https://doi.org/10.1109/CCPIS59145.2023.10291780

2. D. Jena, S. Das, E. Mohapatra and **T. P. Dash**, "Effect of Nitride Stress on Linearity performance of AlGaN/GaN HEMT," 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), Kolkata, India, 2022, pp. 115-118. doi: https://doi.org/10.1109/EDKCON56221.2022.10032924

3. D. Jena, **T. P. Dash**, N. Sahoo, A. K. Sahu, A. K. Panda and T. Sahu, "Improvement of Transport Mobility in Asymmetric V-shaped Double Quantum Well Structure," 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), Kolkata, India, 2022, pp. 156-159. doi: https://doi.org/10.1109/EDKCON56221.2022.10032965

4. Mohapatra, D. Jena, S. Das, J. Jena and **T. P. Dash**, "Work-Function Variability impact on the performance of Vertically Stacked GAA FETs for sub-7nm Technology Node," 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), Kolkata, India, 2022, pp. 440-444.
doi: https://doi.org/10.1109/EDKCON56221.2022.10032850

5. Jena, S. Das, E. Mohapatra, S. Choudhury and **T. P. Dash**, "Simulation of GaN-Based Polarization Junction Super HFET for Power Electronics Application," 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), Kolkata, India, 2022, pp. 302-306. doi: https://doi.org/10.1109/EDKCON56221.2022.10032828

6. **T. P. Dash**, C. K. Maiti and D. Jena, "Partially Depleted Silicon-on-Insulator (PDSOI) MOSFETs for RF Switching Applications," 2022 IEEE VLSI Device Circuit and System (VLSI DCS), Kolkata, India, 2022, pp. 89-92, doi: https://doi.org/10.1109/VLSIDCS53788.2022.9811445.

7. Devika Jena, **T. P. Dash** S. Das, E. Mohapatra J. Jena and S. Choudhary, "Simulation of Recessed Gate Pseudomorphic AlGaAs/InGaAs/GaAs HEMT for RF Applications" 6th International Conference on Devices, Circuits and Systems (ICDCS) 2022. https://doi.org/10.1109/ICDCS54290.2022.9780836

8. E. Mohapatra, **T. P. Dash**, S. Das, J. Jena, J. Nanda and C. K. Maiti, "Investigation of Work Function Variation on the Electrical Performance of sub-7nm GAA FETs," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 103-106, DOI: https://doi.org/10.1109/DevIC50843.2021.9455911

9. J. Jena, S. Das, E. Mohapatra, J. Nanda and **T. P. Dash**, "Performance Analysis of FinFET based inverter at 7nm Technology Node Using TCAD Simulation," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 143-147, DOI: https://doi.org/10.1109/DevIC50843.2021.9455817

10. **T. P. Dash,** E. Mohapatra, S. Choudhury, B. Jena and C. K. Maiti, "Strained SiGe Channel TFTs For Flexible Electronics Applications," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 355-358, DOI: https://doi.org/10.1109/DevIC50843.2021.9455788.

11. S. Das, E. Mohapatra, S. Choudhury, **T. P. Dash** and C. K. Maiti, "Stress-Engineered AlGaN/GaN High Electron Mobility Transistors Design," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 471-473, DOI: https://doi.org/10.1109/DevIC50843.2021.9455852

12. D. Jena, E. Mohapatra, F. A. Ali and **T. P. Dash**, "A Simulation Study of 2-D Electron Gas in GaN HEMT for High- Speed Applications," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 411-415, DOI: https://doi.org/10.1109/DevIC50843.2021.9455878

13. S. Das, A. Raju, **T. P. Dash**, "Geometry dependent RF performance of FinFETs," 2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT), 2021, pp. 1-4, doi: https://doi.org/10.1109/APSIT52773.2021.9641234

14. R.M. Asif, S. U. Rehman, A. U. Rehman, M. Bajaj, S. Choudhury, and **T. P. Dash**, "A Comparative Study of Short Channel Effects in 3-D FinFET with High-K Gate Di-electric," *2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT)*, 2021, pp. 1-5, doi: https://doi.org/10.1109/APSIT52773.2021.9641388.

15. D. Jena, S. N. Das, **T. P. Dash**, and F. A. Ali, "High-Speed MAC using Integrated Vedic Mathematics High-Speed MAC using Integrated Vedic Mathematics," 2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT), 2021, pp. 1-4, doi: https://doi.org/10.1109/APSIT52773.2021.9641235.

16. J. Jena, **T. P. Dash**, E. Mohaptra, S. Das, J. Nanda and C. K. Maiti, "Performance Analysis of FinFETs with Strained-Si Fin on Strain-Relaxed Buffer," 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), 2020, pp. 327-330, DOI: https://doi.org/10.1109/VLSIDCS47293.2020.9179862

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18. F. A. Ali, **T. P. Dash**, D. Pradhan, and G. Bose, "Comparison study of GaSb and Strained-Si p-MOSFETs," 3rd International Conference on Electrical, Electronics, Engineering trends, Communication, Optimization and Sciences (EEECOS)-2016, pp. 1-5, 2016. DOI: https://doi.org/10.1049/cp.2016.1545

19. E. Mohapatra, **T. P. Dash**, J. Jena, S. Das and C. K. Maiti, "Performance Analysis of Sub-10nm Vertically Stacked Gate-All-Around FETs," 2020 IEEE VLSI DEVICE CIRCUIT AND

SYSTEM (VLSI DCS), 2020, pp. 331-334, DOI: https://doi.org/10.1109/VLSIDCS47293.2020.9179913

20. **T. P. Dash**, S. Das, S. Dey, E. Mohapatra, J. Jena, and C. K. Maiti, "SPICE Parameter Extraction of Tri-Gate FinFETs- An Integrated Approach," in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 291-294,2019. DOI: https://doi.org/10.1109/DEVIC.2019.8783725

21. S. Dey, J. Jena, **T. P. Dash**, E. Mohapatra, S. Das, and C. K. Maiti, "Performance Evaluation of Gate-All-Around Si Nanowire Transistors with SiGe Strain engineering" , 2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), 2019. DOI: https://doi.org/10.1109/MOS-AK.2019.8902440

22. S. Dey, **T. P. Dash**, S. Das, J. Jena, E. Mahapatra, and C. K. Maiti, "Variability Due to Orientation Dependent Oxide Thickness in SOI-FinFETs," 2018 IEEE Electron Device Kolkata Conference (2018 IEEE EDKCON), pp. 152-156, 2018. DOI: https://doi.org/10.1109/EDKCON.2018.8770390

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24. **T. P. Dash**, S. Das, D. Pradhan, and S. Dey, "Investigation of low temperature performance in heterostructure Strained-Si n-MOSFET," 2017 2nd IEEE International Conference on Man and Machine Interfacing (MAMI 2017), pp. 1-6, Dec 2017. DOI: https://doi.org/10.1109/MAMI.2017.8307884

25. S. Dey, **T. P. Dash**, S. Das, and C. K. Maiti, "Performance Prediction of SOI FinFETs in the Presence of Random Discrete Dopants," 2018 IEEE International Symposium on Devices, Circuits and Systems, pp. 1-4, 2018. DOI: https://doi.org/10.1109/ISDCS.2018.8379640

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27. C. K. Maiti, S. Das, and **T. P. Dash**, "Assessment of Heterojunction SiGe Tunnel-FET for Low-Power Digital Circuits," in IEEE International Conference on Device Integrated Circuits (DevIC-2017), pp. 336-340, 2017. DOI: https://doi.org/10.1109/DEVIC.2017.8073964

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30. **T. P. Dash**, S. Dey, J. Jena, S. Das, E. Mohapatra, and C. K. Maiti, "Metal Grain Granularity Induced Variability in Gate-All-Around Si-Nanowire Transistors at 1nm Technology Node," in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 286-290, 2019. DOI: https://doi.org/10.1109/DEVIC.2019.8783717

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